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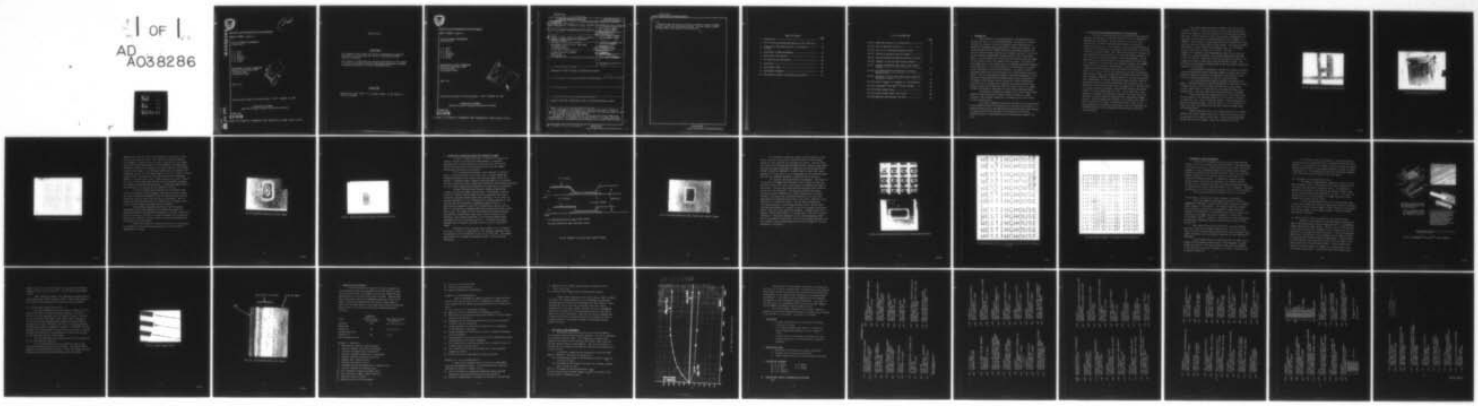

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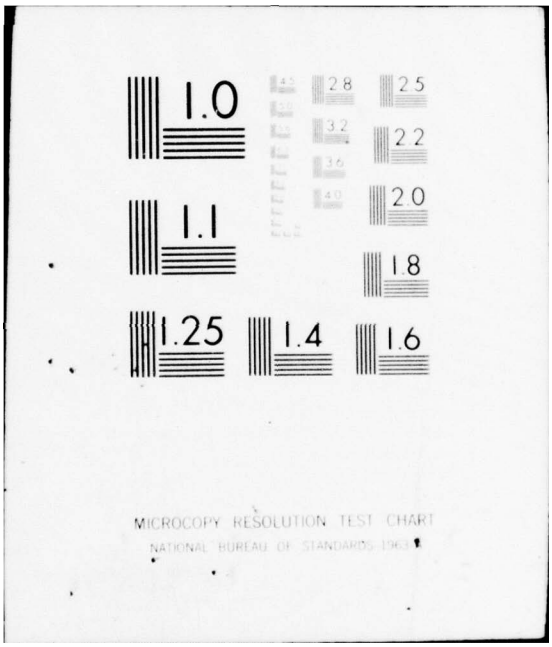
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Research and Development Technical Report

Report ECOM-72-0061-10

THIN FILM TRANSISTOR-ADDRESSED DISPLAY DEVICE

T. P. Brody
F. C. Luo
D. H. Davies
E. W. Greeneich
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APRIL 1977

Tenth Quarterly Report for Period October 1, 1974 - December 31, 1974

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PREPARED FOR:

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US ARMY ELECTRONICS COMMAND FORT MONMOUTH, NEW JERSEY 07703

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The achievement of operational 6 x 6 inch 30 lpi dot matrix displays is reported. The addressing is accomplished using thin-film transistor matrices and the display medium is ac-electroluminescence

The panel was operational over all its area but the quality needs to be improved before it is comparable to the near perfect 20 lpi panels fabricated. A good method for interconnecting was developed using a solder bonded PC board.

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Greater than 75% active lit area was achieved on several displays through a second level electroding process. Further progress towards improved defect free operation can be expected.

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1. INTRODUCTION

The objective of this program phase is the demonstration of a 30 lines per inch, 6 x 6 inch TFT-EL display. The device will further validate the concept of thin film transistor matrix addressing as a method for integrated signal distribution in solid state display. The 30 lpi display contains ∿30,000 individually addressable elements and, with two transistors and a capacitor per element, results in a thin film matrix containing ∿60,000 TFTs, 30,000 capacitors and a three busbar matrix. At first glance this looks like a very difficult goal but based on our results to date it is readily within our grasp. The reason for this anomaly lies in the unique nature, but somewhat unfortunate semantics, in the TFT itself. In fact the problem is the fabrication of a single, albeit multi-level, thin film active matrix. All these so called individual devices are no more than parts of a simultaneously fabricated matrix. Thus the large apparent number of individual components is illusory and to take individually determined failure rates and multiply by the number of TFTs is not a correct method for failure determination. In practice we are dealing with a single active matrix that will have indeed a certain failure mode but this will differ little if the number of TFTs is increased or decreased, all other factors remaining equal.

We therefore introduce the concept of the "active matrix" which unlike its near relation the "passive matrix" provides for element isolation, frame refresh storage and, if necessary, grey level control at every picture point.

This report summarizes the results obtained in the second quarter of the program devoted to the fabrication of the 30 lpi active matrix. In addition further data on the fabrication yield problems with these displays is presented and a brief discussion of some minor, but difficult, related problems in interconnection and in increasing the element "lit' area.

2. THIN FILM DISPLAY FABRICATION RESULTS AT 30 LINES/INCH

The basic design and fabrication techniques having stayed the same with the increase in resolution from 20 to 30 lpi no significant problems were anticipated. This has been the case but our recent experience has revealed that process modification is necessary to achieve good TF circuits. The increase in limiting tolerance showed up clearly in an increased level of elemental shorted devices. This is due to TFT gate overlap problems. More than minimal overlap of the gate over the source-drain electrode results in a great percentage increase the total "capacitor" surface area subject to voltage breakdown. This is much more critical than the busbar or storage capacitor overlap since it is impossible to increase the gate insulator thickness (now $\sim$5000Å) without loss of transistor transconductance. The problem is more acute for the 30 lpi display since the tolerances are smaller, the ability of X-Y jig to control the tolerances is the same as previously while the total number of overlaps (four per double gated TFT) increases from $\sim$100,000 to $\sim$250,000. A detailed analysis of the problem indicated that an improvement in pattern registration between separate steps was achievable through more careful sequencing of the deposition steps. In particular, since the shifts that occur are largely due to thermal effects in the jig, substrate, and mask, care was needed regarding the thermal history of the "as depositing" TF circuit. It was found that it was important to deposit the bottom gate, the source and drain and the top gate under conditions where the substrate had a reproducible thermal history. The best results were obtained if the substrate was "cold" at each of these critical steps. The principal source of heat is the Al_2O_3 deposition; an increased cooling period after this deposition was initiated with the critical components then consistently deposited after this step.

The improved gate/source:drain location at the 30 lpi level is shown in Fig (1). Since this long cool period could slow the cycle time in any commercial fabrication process it is potentially an undesirable step. Two alternatives to avoid this have been investigated. The first was very fast rates of insulator deposition (up to 50Å/sec from ~5Å/sec). The increase in e-beam evaporation hearth temperature is quite small but the total thermal input is much reduced. This approach worked but results in poorer control over deposition rates, not a desirable factor at this critical stage in the venture. The other approach is to backfill the vacuum system with pure, dry nitrogen and "flush" it for several minutes. The clean gas ensures fast pump down to the 10^{-7} mm Hg range and the gas allows conductive cooling to the chamber walls which is much faster than the radiative cooling. This method has been conclusively demonstrated and has been used at appropriate intervals in the process.

Other procedures implemented to improve the tolerance standards included reworking the pattern coordinate numbers to ensure that the jig allows the operator to approach the appropriate setting from the same direction, and recabling the jig to take out off-axis tensions.

To prevent scattering of material between the substrate and mask, a limiting constraint on pattern separations in thin film circuitry of high resolution, the jig settings were modified to ensure every critical pattern edge is created with the top (substrate) mask as the defining side. This also helps device reproducibility and uniformity.

These approaches have allowed good pattern fabrication but as yet the quality of the resulting displays is not as great as achieved at the 20 lpi level. Fig (2) shows one example of partial operation and Fig (3) an improved display. Note that several of the line defects in Figs (2,3) arise from problems with the edge connection scheme; these are discussed below.

Another problem met with at the higher resolution is concerned with the inter-level laminar resist used to isolate the circuitry from the EL layer in the inactive circuit area. This process was described earlier for the 20 lpi display. Since the EL contact pad is now

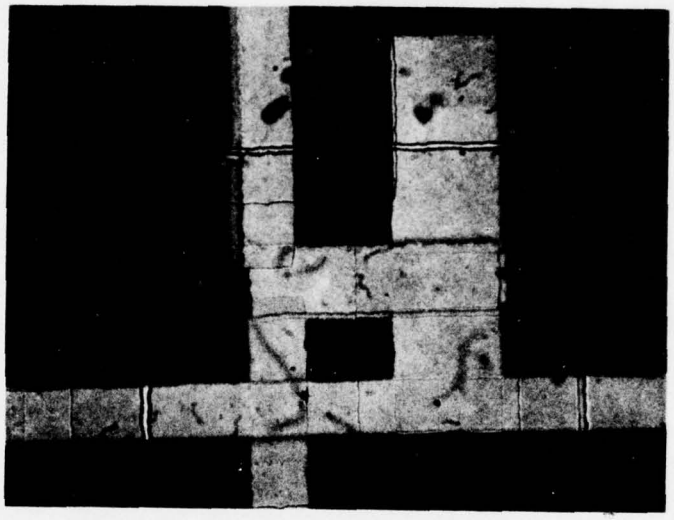


FIG (1) Good Gate Overlaps in TFT Fabrication

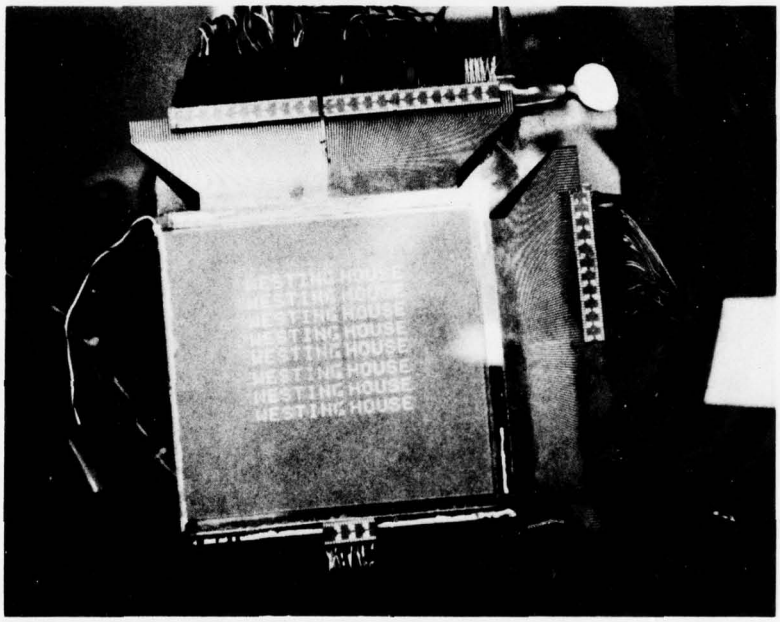


FIG (2) Partial Operation at 30 lpi

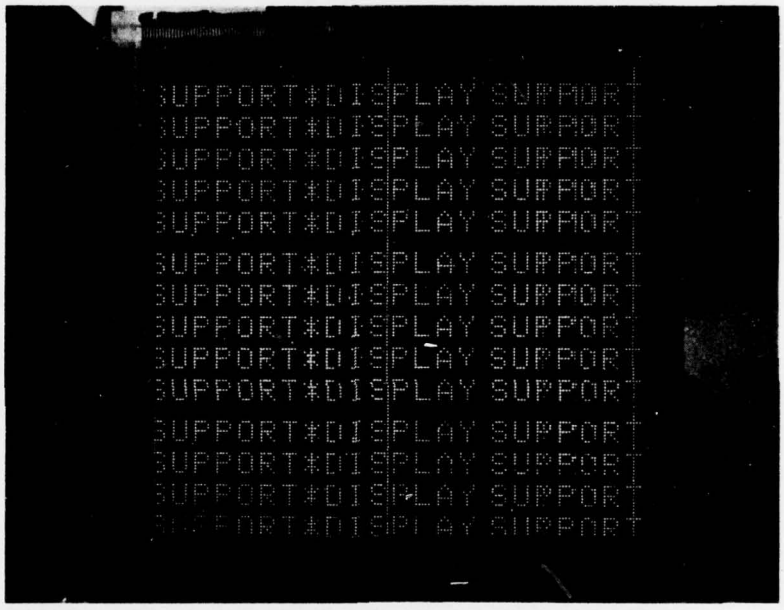


FIG (3) Best 30 lpi Performance Achieved to Date

significantly reduced in size, the reliability of the contact to the EL layer was found to be poor. This results in inoperable elements even though the elemental circuit is good. Examination of the coated circuits with pad areas opened up in the photoresist developing steps, showed poor removal of the resist in the contact region. Fig (4) shows a typical poor sample of an individual element having the aperture not adequately cleared out. The simple answer to this is of course to develop longer, however this results in poor edge definition and inadequate adhesion in the photoresist layer. Many processes were tried to improve this but the final answer came from the use of professional equipment for exposure, laminating and developing. A simple hand rigged approach had worked well at 20 lpi but was not adequate at 30 lpi.

A "Colite" laminar resist exposure unit and a DuPont spray developer and laminator were purchased. With care these have allowed us to more uniformly and adequately form the isolation level with good electrical contact at each of the picture point apertures. Fig (5) illustrates the improved process, the cleaner etch out, without loss of overall aperture diameter and edge quality is obvious.

The performance demonstrated in Fig (2) and (3) require improvement but more than adequately proves that the concepts and methods developed in this program are extendable to 30 lpi. Indeed from the TF circuit point of view we can readily envisage that even greater densities are achievable. Further progress in process optimization can be expected in the next quarter.

No major TFT electronic problems were met with in this period; the transistors, both logic and power switch have proved reliable, reproducible and stable.

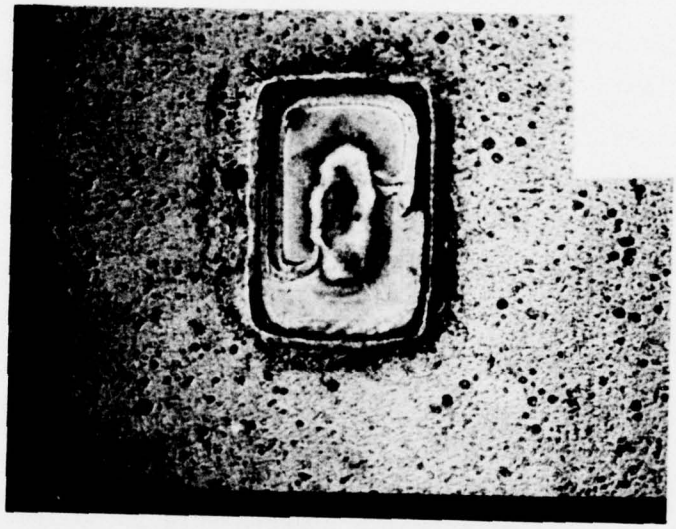


FIG (4) Photoresist Aperture not Fully Opened

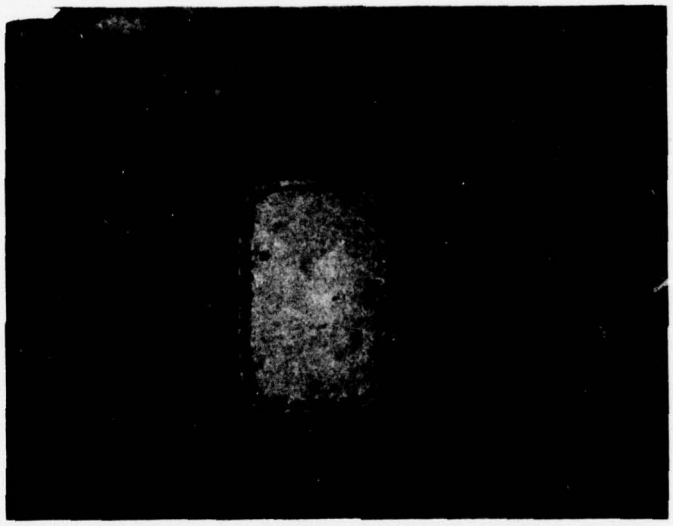


FIG (5) Improved Photoresist Aperture Clean-out at 30 lpi

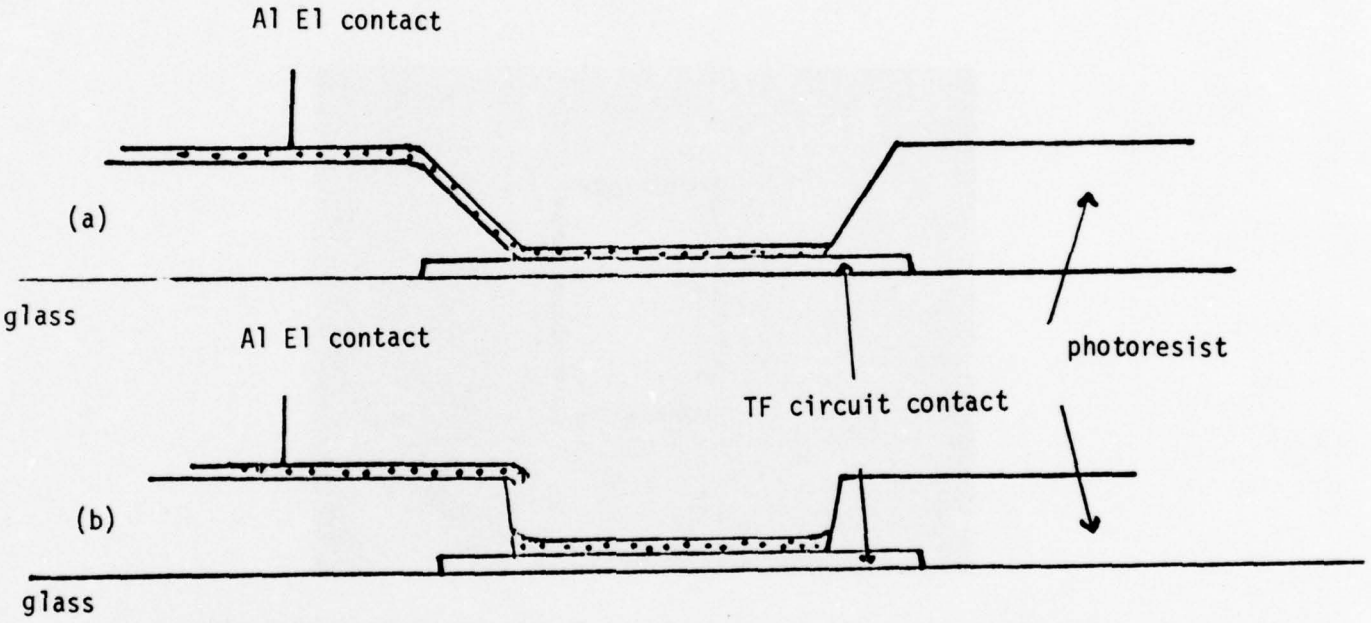
3. SECOND-LEVEL ELECTRODING PROCESS FOR INCREASED LIT AREA

In order to increase the active or percent "lit" area of the display a second level process has been proposed. As explained previously this involves extention of the EL pad over the thin film circuit area with electrical isolation preserved using the laminar photoresist already used in the process.

Our first problem was related to that described in Section 2 above; viz clean apertures in the contact area. Similar methods and processes described in that section were used and largely solved this problem. In addition several chemical etches described in the literature for this purpose were tried, in particular bisulfites. These materials,developed for the PC board industry were ineffective for these thin film substrates.

The major difficulty met with was forming and maintaining reliable contact at the edge of the aperture. This problem, clarified in Fig (6), results from the inability of the evaporated thin films to effectively penetrate around corners with continuity. If the resist is properly developed, i.e. it is ensured that no residual material is left, then the edge of the aperture is overhung as shown in Fig (7). In depositing the electrode it will fail to bridge and no contact will be made. If the aperture is underdeveloped then of course the overall contact will be poor. An attempt to solve this problem with rf sputtering was unsuccessful; although better edge contact could be achieved it was difficult to get uniform distribution of top electrode metallization (aluminum) over this relatively large area. In addition the pattern sharpness was not adequate, good pad isolation being of course still needed.

Evaporation at an acute angle was attempted, i.e. the treated TF circuit is placed at a sharp angle to the aluminum evaporation source. The substrate is then turned 180° to pick up the other side. This method proved difficult to adequately implement and gave very non-uniform thicknesses.



(a) graduated photoresist edge; allows contact

(b) sharp photoresist edge; contact not formed

FIG (6) Schematic of the Two Level Contact Problem

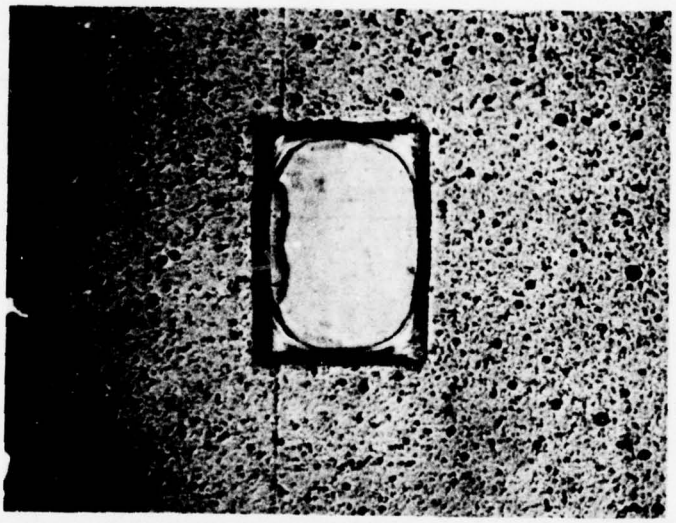


FIG (7) Overhung Photoresist Edge, Double Level Contact Problem

An alternative concept was tried; the opened aperture in the resist layer was screened with a conductive paste so that the paste filled the entire aperture and "smoothed" the surface. This was tried both with a silk screening aperture mask and with a simple wiping method. The electrode pattern was then over deposited over the conductive ink. Another alternative consisted of a double layer of resist with larger openings in the top layer to act as receptacles for the conductive paste. This was too cumbersome and messy a method and was not effective.

The eventual optimal approach was the simplest. The phototool for aperture development was fabricated in the X-Y mask jig with less than hard vacuum ($\sim 10^{-5}$ torr), this resulted in slightly fuzzy edges to the pattern. This was then contact printed onto high quality film and used as the master phototool. This was only partially successful initially but when combined with a careful optimization of exposure intensity, developing time, developing temperature and, after much experimentation regarding holding times on the resist, resulted in near 100% first to second level contact. Fig (8) shows the resulting electroded apertures at various magnification levels. Fig (9) shows the resulting operation in a portion of the 30 lpi display and Fig (10) shows a close up of some operational elements. Although further work is needed to improve the process it is evident that it will work with good reliability. Subjective examination of the resulting displays shows that the increased lit area (now $\sim$ 75% of total available elemental area) has a dramatic effect towards improving the overall legibility and area brightness of the device.

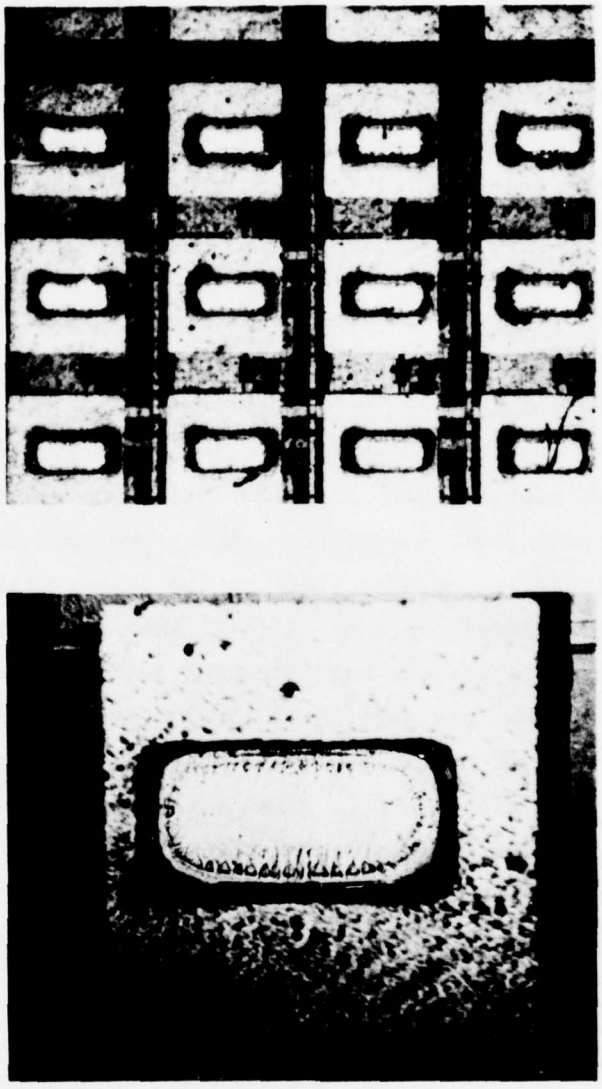


FIG (8) Electroded Second Level Apertures at Various Magnifications

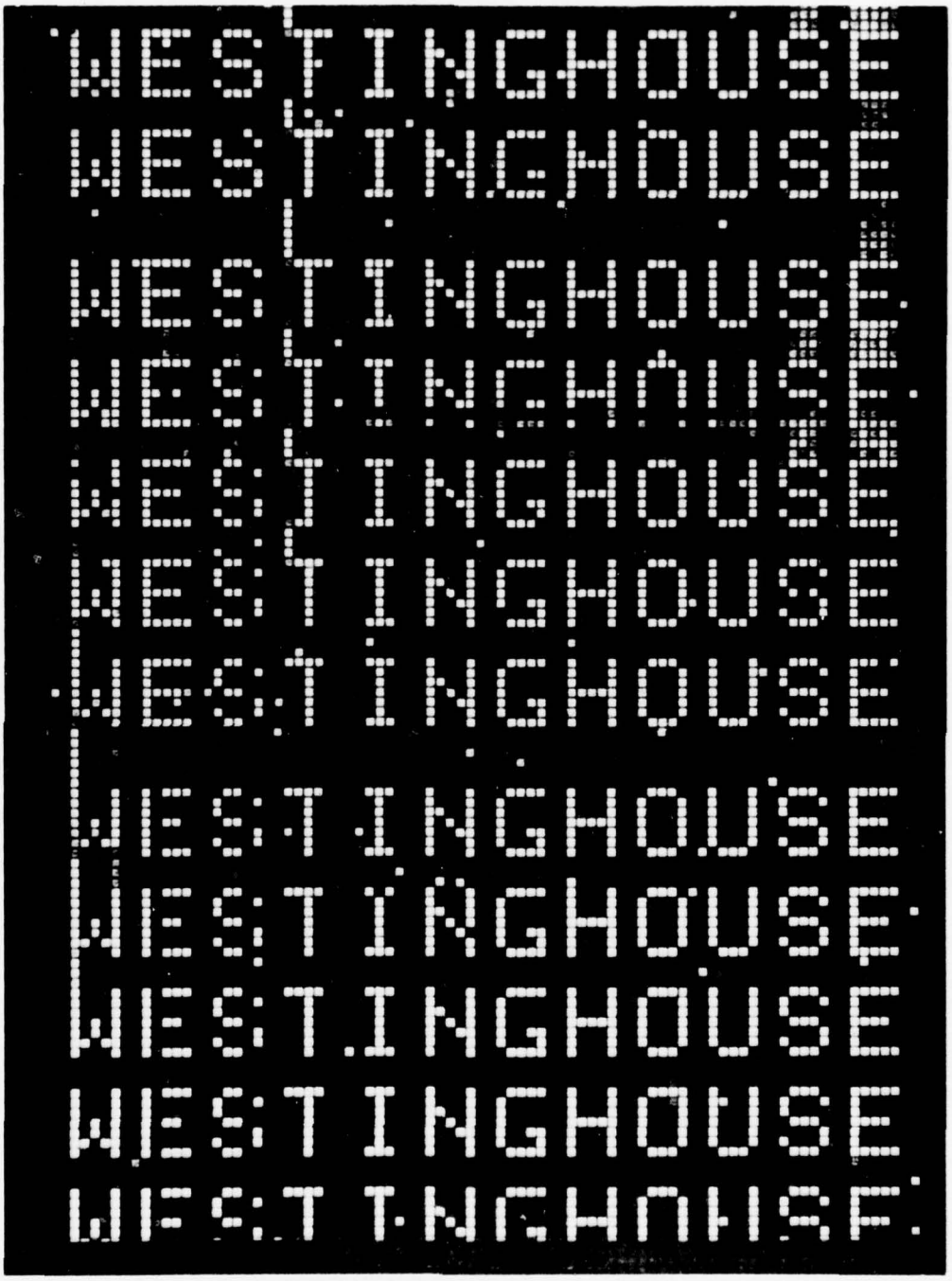


FIG (9) Operation at 30 lpi with Second Level Process for Increased Lit Area

FIG (10) Further Example of Increased Lit Area Operation

4. INTERCONNECT SCHEME DEVELOPMENTS

The ability to reliably connect the 30 lpi evaporated edge fingers to the drive circuitry is an interim problem of some significance. It is interim in that the eventual objective of the overall TFT display program is a fully integrated display with peripheral shift register deposited co-extensive with the matrix pattern. Until this is achieved however a method has to be found to connect to the output of the exerciser described previously. No commercial connectors having a density greater than 20 lpi are available. The connector must be reliable with a relatively low contact resistance and must,preferably, be easily made and broken repeatedly without loss of integrity. Individual wire bonding is out of the question with the circuits of this complexity.

Four approaches have been examined in detail, as follows;

(a) Elastomeric contacts with discrete elements and redundancy

These new commercial developments are based on a strip of compressible elastomeric core having electrically conductive circumferential fingers at a high density. Two separate commercial products, both it should be noted in their developmental stage, were tried, (i) AMP Inc "elastomate$^{(R)}$, a compressible strip having a plastic film overlay with gold beads around the circumference, see Fig (11), (ii) Technit "Zebra"$^{(R)}$ connector. This material is also compressible but has carbon impregnated layers interspersed with insulator layers. See Fig (11).

Both these materials were tried using a jig that held the panel and a fabricated polyimide/copper fan out. This fan out (from 30 lpi to 20 lpi) was made using conventional PC board techniques, 1 oz copper clad Kapton, and a photopattern generated with the "Applicon"$^{(R)}$ CAD system.

The elastomeric material is placed between the copper fan out fingers and the evaporated panel fingers. Crude alignment is needed between the contacts. The inserted material has multiple redundancy in the contacts so that exact alignment is not needed. This also acts to improve reliability.

Both methods require even pressure to be exerted and this was achieved with a screw mounted bar. Problems were found with this approach; the reliability of the contacts was not good with our methods and the poor uniformity of the pressure resulted in regions of uneven compressibility. The consequence was shorting and material breakdown in the tight places and no contact in the loose region.

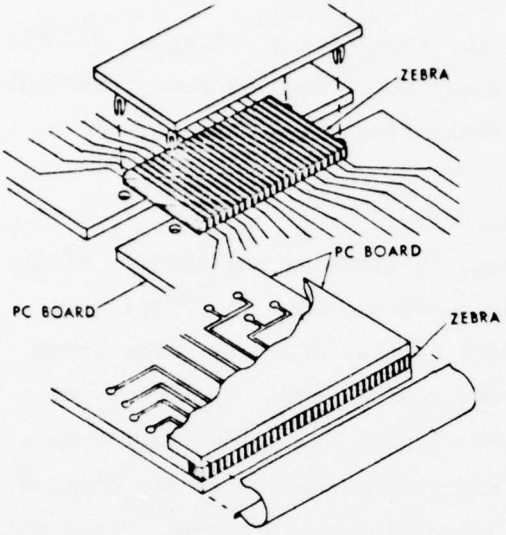
(b) Elastomeric with non-discrete contacts

The Chomerics Company make an elastomeric contact that has many thousands of metal filled matrices that, when compressed across the layer, short and form a continuous contact. No alignment is needed with this method. This material was examined using the same fan out, jig and panel method described in (a) above. Once again the reliability was not good and element to element shorting occurred together with regions of poor contact.

It was concluded that both (a) and (b) would probably work but that they required more elaborate jigging and technique development on our part. For the limited number of panels required in this program this was not thought to be an optimal solution. Further techniques were therefore examined.

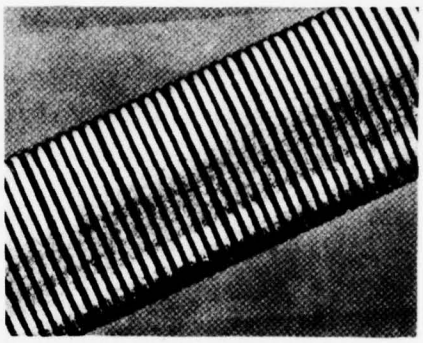
(c) Direct fan out contact on plated and solder dipped fingers

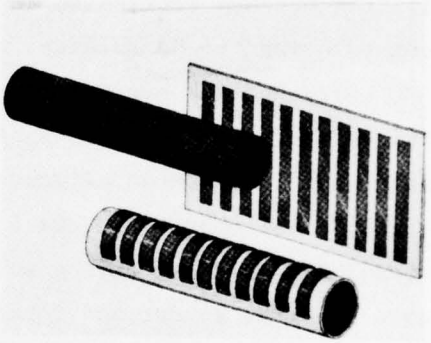
Building on the previous fan out development an attempt was made to make good pressure contacts <u>directly</u> between the copper/Kapton fingers and the panel edge contacts. This of course is made difficult by (i) the need to get exact alignment with the fingers, and (ii) the difficulty in obtaining low contact resistance. The first problem was minimal with care and skill in the alignment process being exercised. The second problem required significant development. Several methods to electrolytically and electrolessly deposit gold and copper on the panel fingers were tried with some success. A better approach was carefully controlled solder pot dipping of the display panel into a low melting indium solder. A rosin free process was developed that



The "Zebra" concept (top) features alternate layers of conductive and non-conductive rubber.

"Zebra," filled elastomer connectors manufactured by Technical Wire Products Inc., Cranford, N.J.





The AMP Elastomate Connector is a unique and extremely simple, yet reliable, connector which fulfills the requirement to interconnect microminiature devices by pressure alone, without the necessity for soldering, bonding, or large space-consuming connector bodies and associated hardware.

FIG (11) Elastomate(R) and Zebra(R) Contact Methods

depended largely on clean panel fingers of an appropriate material; chrome-gold was found to be the best. Fig (12) shows solder dipped fingers.

When compressed together, the copper/Kapton fingers and the panel fingers made a fairly reliable contact. However some lines out in the panel clearly indicated the limitations with this method.

(d) Solder bonded contacts with overlay

The best temporary solution, in terms of reliability of the contact, was found to a direct solder-bond process. A 20 lpi to 30 lpi fan out was fabricated on stiff regular PC board. The board is cut to bring the board edges to the contact edge. Both ends of the PC board and the evaporated panel fingers are solder dipped as described in (c) above. The panel and the fan out board are abutted together with as good an alignment as possible. A Kapton(R) film with straight 30 lpi copper fingers is placed over both contacts to overlay the panel and then fan out. A soldering iron is moved over the film to melt down the solder and form the bond.

Fig (13) illustrates the resulting contact and the panel with fan out is illustrated in Fig (2).

An alternate method was to use conductive epoxy to bond individually between the fan out and the panel. This method, while effective, was laborious and was subject to shorting between the lines. Nevertheless several panels were fabricated with this method.

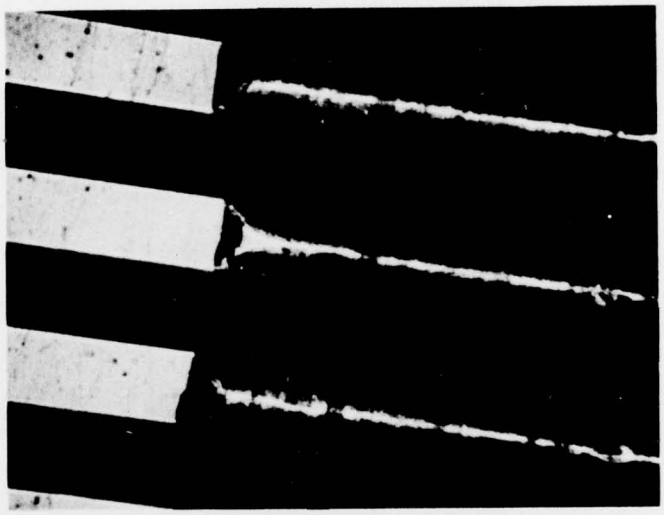


FIG (12) Solder Dipped Fingers

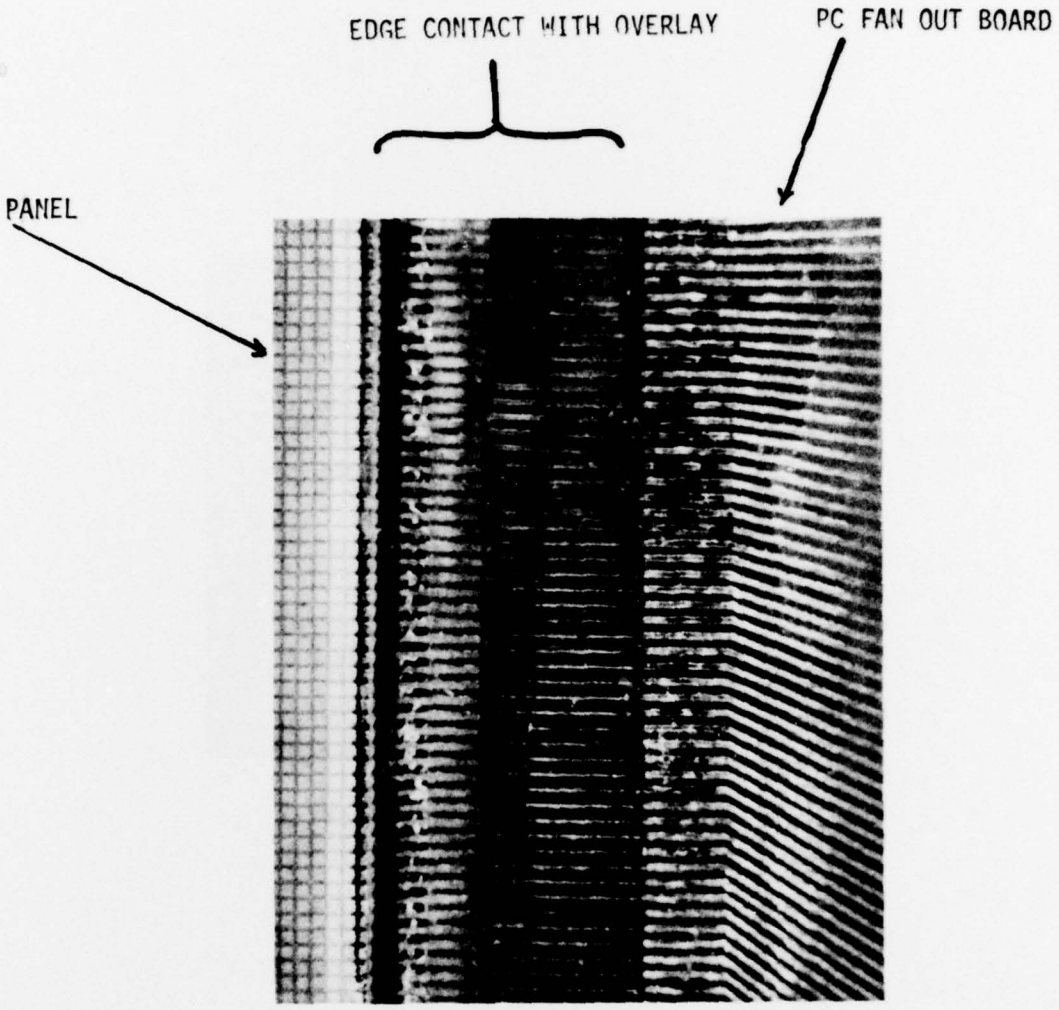


FIG (13) Solder Bonded Contact with Overlay

5. FABRICATION YIELD ANALYSIS

A detailed analysis of fabrication yield, as applied to this laboratory process, was presented in the last quarterly report. There the major sources of incomplete "starts" were identified and the pivotal role of the TFT circuit plate clarified. However about 25% of the scrap is due to the subsequent processing of the circuit plate. This has been analyzed and the overall results shown in Table (1); this data applies to the single level process only and also does not take into account the interconnect problem discussed in Section 4.

TABLE (1)

Class	Percent of total attributable	Major items in order of importance
Category I Human Error	55%	8, 4, 9, 11, 14, 16
Category II Process malfunction	35%	17, 20, 23, 24
Category III True irreproducibility	10%	27, 29

Category I - Human Error

1. Edge connector mask not aligned properly
2. Incorrect exposure time used in photoresist
3. Incorrect developing time in photoresist
4. Incorrect alignment of phototool in photoresist
5. Phosphor spray mix formulated incorrectly
6. Phosphor spray timing incorrect
7. Filming spray timing incorrect
8. Inadequate drying time-temperature of phosphor layer
9. Incorrect sequence in spray/dry steps
10. Poor shielding of edges in phosphor spray
11. Poor shielding of edges in gold evaporation
12. Edge wire contact not made
13. Epoxy catalyst incorrectly measured

14. Epoxy cure incorrectly timed
15. Top seal plate mislocated
16. General breakage due to mishandling

Category II - Process Malfunction

These are problems not readily classified as human error but include those factors that are due to inadequacy in process control. It is assumed that the nominal process specification was followed in all these.

17. Poor "clean out" of photoresist apertures
18. Adhesion failure of photoresist in subsequent processes
19. Minor defect in photoresist arising from "bubbles" or other inherent defects in the material
20. Misregistration of photoresist mask with TF circuit electrode due to mask or pattern distortions
21. Voltage breakdown in resist during operation due to "thinning" of the material in developing
22. Voltage breakdown in the EL layer (too thin); arising from process control inadequacy
23. Low brightness in the EL layer (from too thick a phosphor/film layer) arising from process control inadequacy.
24. Poor conductivity in gold top electrode due to residual solvent in EL layer despite good dry cycle.
25. Poor conductivity in gold top electrode due to poor vacuum in evaporation process.
26. Poor EL life due to high humidity in panel seal step.

Category III - True Irreproducibility

These are the variables that are as yet not identifiable and cause unassignable problems. It is anticipated that these will eventually be reduced to Category II or I.

27. Lack of uniformity in operational brightness despite good TFT uniformity and subsequent process within specification
28. Patches of unmodulatable lit phosphor in surround of "active" pads

29. Regions of "off" elements despite positive indication in TF circuit panel test.

30. Completely dead display despite nominally good process.

Despite this extensive list of trouble spots, common it should be noted to all complex processes, it is encouraging that hard and fast identification of most of the variables has been achieved. These variables are for the most part correctable given time, effort, standardization, and some training. Further the as yet unassignable problems are probably due to poor observation and are in fact due to human error not yet detectable. These are all typical variables that a production process can clarify and control; the degree of control already achieved is very hopful in terms of anticipated eventual production yields.

6. TFT STABILITY AND PERFORMANCE

The astable multivibrator test has continued and 6000 hrs of continuous pulsed operation has been obtained. The test is described in the eighth quarterly report. As of 6000 hrs no change in TFT threshold, as measured by the sensitive multivibrator pulse interval, has been observed since the last 3500 hrs. Thus since the start of the test the total change in pulse period is 8% and the threshold shift is only 0.2 volt.

In Fig (14) is shown the data pertaining to the first 6000 hours of operation. Plotted in the figure are:

(1) the percentage change in the multivibrator period (ΔT_{MVB}) as a function of time,

(2) The change in TFT threshold voltage (ΔV_T), showing a maximum shift of 0.2-0.3 volts,

and (3) the change in TFT transconductance (Δg_m).

It is to be noted that the small change in g_m(2%) is a result of the 0.2 volt shift in threshold voltage.

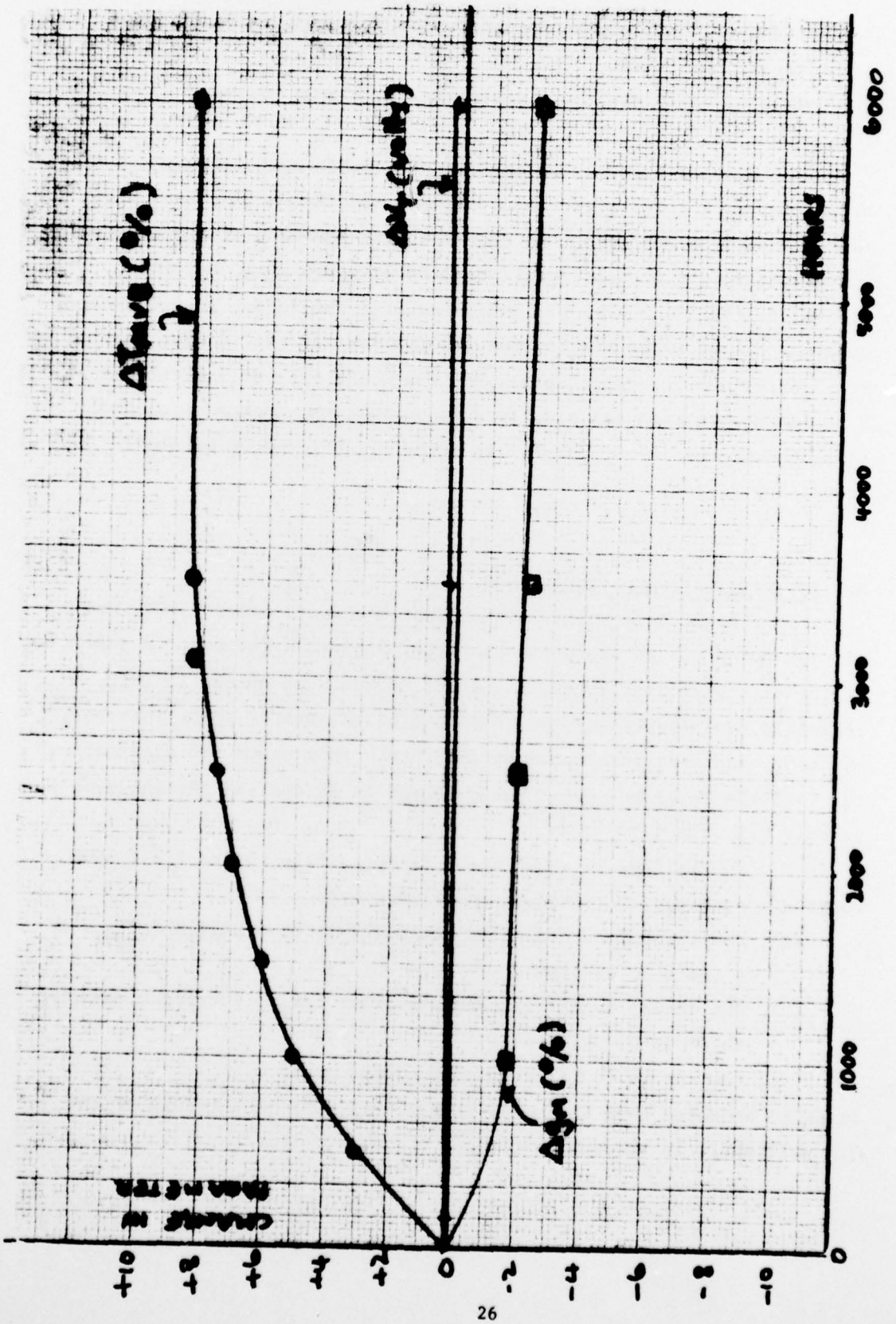


FIG (14) 6000 Hour Multivibrator Test Data

Instabilities in insulated-gate field-effect transistors are the result of electronic trapping and/or the migration of ionic species. Vacuum deposited thin-film transistors, fabricated entirely within the vacuum system, do not exhibit ionic instability, unless deliberately contaminated. On the other hand silicon MOS devices, by necessity, are exposed to ionic contaminants during fabrication. As a result it took many years and considerable effort for the silicon MOS industry to bring MOSFET instabilities under reasonable control.

The measured 6000 hr change is not only small compared to equivalent silicon devices,but,most important,is insignificant in regard to the operation of the display. This test is continuing.

7. CONCLUSIONS

1. No major difficulties have been found in increasing resolution to 30 lpi.
2. It is however somewhat more difficult to obtain low defect, high quality displays at 30 lpi compared to 20 lpi.
3. A good process for increasing the elemental lit area has been developed; it vastly improves the subjective legibility.

8. NEXT QUARTER PLANS

1. Good defect free single-level displays fabricated
2. Reliable second level process developed
3. Further characterization on display properties obtained

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